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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/611,791	06/30/2003	Xiaoning Ye	42P15581	1296

8791 7590 09/10/2004

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EXAMINER	
NATALINI, JEFF WILLIAM	

ART UNIT	PAPER NUMBER
2858	

DATE MAILED: 09/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/611,791	YE ET AL.	
	Examiner	Art Unit	
	Jeff Natalini	2858	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-13,15-21,23 and 24* is/are rejected.

7)☒ Claim(s) *7,14,22 and 25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 11 and 16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In regard to claim 11, the limitation "the signal trace anti-pad region" is recited in line 2 of the claim. There is insufficient antecedent basis for this limitation in the claim. The claim will be examined as though this part is removed.

In regard to claim 16, the limitation "the signal" is recited in line 1 of the claim. There is insufficient antecedent basis for this limitation in the claim. The claim will be examined as though a signal was introduced in this claim.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 8, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Govind et al. (6531932) in view of Klaassen (5608591).

In regard to claims 1, 8, and 23, Govind et al. discloses a multilayer substrate/test structure/method (abstract-2nd sentence) comprising: at least one signal trace disposed on a dielectric layer (col 3 line 17-22), wherein the trace comprises a first width that is wider then a second width (abstract last sentence); and a via attached to the trace (col 1 line 24-27); a component attached to the via wherein a impedance discontinuity between the at least one signal trace and the component is lowered (col 3 line 45-48; it is known in the art and would be inferred that via is used when attaching a component to a trace in a multilayer board).

Govind et al. does not specifically disclose a via attached to the first (wider) width connected to the via.

Klaassen teaches that some areas in an electrical traces change dimensions depending on certain factors, and one such changes would be to vary the width to accommodate for the greater width of bonding areas (col 3 line 36-48; it is known in the art bonding areas contain vias among other things).

It would have been obvious to one with ordinary skill in the art at the time the invention was made for Govind et al. to specifically attach at via to the wider width as taught by Klaassen in order to compensate for changes in the characteristic impedance (col 3 line 36-42).

5. Claims 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Govind et al. (6531932) in view of Klaassen (5608591) as applied to claim 8 above, and further in view of Arabi (6501278).

Claims 18 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Govind et al. (6531932) in view of Klaassen (5608591), and further in view of Arabi (6501278).

In regard to claims 15-17, Govind et al. and Klaassen do not specifically disclose wherein the component is adapter for receiving a signal of above 5 Gigahertz; and wherein a signal is launched through a prober and a signal output is coupled to the component.

Arabi provides a matching impedance between the probe tip and the circuit board trace (abstract); a signal is provided into the circuit board, and a reflection is received back, thus being a signal output (col 1 59-63); TDR can produce a signal between 1-20 Gigahertz (col 7 line 6-11).

It would have been obvious to one with ordinary skill in the art at the time the invention was made for Govind et al. and Klaassen to have a probe to launch a signal and be able to receive the output of the signal as it is reflected back and that signal is above 5 Gigahertz as taught by Arabi in order to have minimal impedance discontinuities at high frequencies (col 3 line 25-27).

In regard to claims 18 and 21, Govind et al. discloses a multilayer substrate/test structure/method (abstract-2nd sentence) comprising: a ground plane formed on dielectric (Fig 1C (16-Vss)); at least one signal trace disposed

on a dielectric layer (col 3 line 17-22), wherein the trace comprises a first width that is wider then a second width (abstract last sentence); a component attached wherein a impedance discontinuity between the at least one signal trace and the component is lowered (col 3 line 45-48; it is known in the art and would be inferred that via is used when attaching a component to a trace in a multilayer board).

Govind et al. does not specifically disclose the component attached to the first (wider) width; and lacks a TDR probing system including a signal output and a signal ground.

Klaassen teaches that some areas in an electrical traces change dimensions depending on certain factors, and one such changes would be to vary the width to accommodate for the greater width of bonding areas (col 3 line 36-48; it is known in the art bonding areas contain vias among other things).

It would have been obvious to one with ordinary skill in the art at the time the invention was made for Govind et al. to specifically attach a component to the wider width as taught by Klaassen in order to compensate for changes in the characteristic impedance (col 3 line 36-42).

Arabi teaches a TDR probing system that includes a signal output and a signal ground (abstract second sentence) for use in circuit board testing (abstract); and teaches the use of a ground pad formed on the first surface of the substrate under test and the ground pad is connected to the ground plane (abstract).

It would have been obvious to one with ordinary skill in the art at the time the invention was made for Govind et al. and Klaassen to have a TDR probing system with a signal output and signal ground as taught by Arabi in order to have minimal impedance discontinuities at high frequencies (col 3 line 25-27).

6. Claims (2, 4, 5, 6), (9, 11, 13), and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Govind et al. (6531932) in view of Klaassen (5608591) as applied to claim (1), (8), and (23) respectively, and further in view of Leddige et al. (6366466).

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Govind et al. (6531932) in view of Klaassen (5608591), further in view of Arabi (6501278) as applied to claim 18 above, and further in view of Leddige et al. (6366466).

In regard to claims 2, 9, 19, and 24, Govind et al. and Klaassen lack wherein the ratio of the first width to the second width is between about 2:1 and 3:1.

Leddige et al. discloses a multilayer circuit board that has a first and second width wherein the ratio is 3:1 (col 3 line 3-9).

It would have been obvious to one with ordinary skill in the art at the time the invention was made for Govind et al. and Klaassen to include the ratio of the first width to the second width to be between about 2:1 and 3:1 as taught by Leddige et al. so that impedance difference between the thick layer and the thin layer are not far mismatched (col 2 line 57-66).

In regard to claims 4, 6, and 11, Govind et al. and Klaassen disclose wherein the signal trace (fig 1C (14)) is located in a ground plane region (fig 1C (16-Vss)).

Govind et al. and Klaassen lack wherein the ground plane regions extends from slightly past the edge of a anti-pad region to where the first width forms; and wherein the first width is not substantially disposed over a ground plane.

Leddige et al. discloses a power and ground planes (fig 5a (30,31)) that are not placed in close proximity to the via (fig 5a (29)), thus providing so the part of the signal trace located near the via is not substantially disposed over a ground plane (30), which is located on both sides of the via a distance away from the via to the end of the trace (fig 5a).

It would have been obvious to one with ordinary skill in the art at the time the invention was made for Govind et al. and Klaassen to have the ground plane region extends from slightly past the edge of a anti-pad region to where the first width forms; and wherein the first width is not substantially disposed over a ground plane as taught by Leddige et al. in order to for the capacitance (which has an effect on the characteristic impedance) to be lower since the power/ground planes are further away from the via (col 4 line 47-52).

In regard to claim 5, Govind et al. and Klaassen disclose a signal trace containing a via (col 1 line 24-27).

Govind et al. and Klaassen lack wherein the signal trace comprises a via pad.

Leddige et al. discloses a via comprising a via pad located on a signal trace (col 5 line 44-46).

It would have been obvious to one with ordinary skill in the art at the time the invention was made FOR Govind et al. and Klaassen to include a via pad for the via on the signal trace in order to couple one signal trace to another (col 5 line 45-46).

In regard to claim 13, Govind et al. and Klaassen lack wherein the component is one of a socket, microprocessor, or a circuit component.

Leddige et al. dislcoses wherein a component attached accordingly is a circuit component (fig 4 (120, 110)).

It would have been obvious to one with ordinary skill in the art at the time the invention was made for Govind et al. and Klaassen to attach a circuit component as taught by Leddige et al. in order to properly use a circuit board to provide electrical signals within electrical components.

7. Claims 3 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Govind et al. (6531932) in view of Klaassen (5608591) as applied to claim 1 and 8 above, and further in view of Downes (6716072).

Govind et al. and Klaassen et al. disclose wherein the signal trace (fig 1C (14)) is located in a ground plane region (Govind et al.-fig 1C (16-Vss)); and wherein the first (wider) width is located close to where the via is formed as disclosed above in reference to claim 1 (Klaassen et al.-col 3 line 36-48).

Govind et al. and Klaassen et al. lack wherein the first width is located in an anti-pad region, wherein the signal trace anti-pad region extends from the center of the via to slightly past the edge of an anti-pad region.

Downes teaches where a via is formed in an anti pad (abstract). It is known in the art the anti-pad region extends slightly past the anti-pad.

It would have been obvious to one with ordinary skill in the art at the time the invention was made for Govind et al. and Klaassen et al. to have a anti-pad containing the via, thus having an anti-pad region around the via, as taught by Downes so that the soldering portion can solder to narrower vias (abstract).

8. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Govind et al. (6531932) in view of Klaassen (5608591) as applied to claim 8 above, and further in view of Pon (4517535).

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Govind et al. (6531932) in view of Klaassen (5608591), further in view of Arabi (6501278) as applied to claim 18 above, and further in view of Pon (4517535).

In regard to claims 12 and 20, Govind et al. and Klaassen lack wherein the component is one of a SMA, BNC, or SIP connector.

Pon teaches using a SMA connector for transferring signals from a signal line device to a circuit board trace (col 10 line 57-61).

It would have been obvious to one with ordinary skill in the art at the time the invention was made for Govind et al. and Klaassen to use a SMA as the

component as taught by Pon in order to connect high frequency signals from a signal line device to a circuit board trace (col 10 line 60-61).

Allowable Subject Matter

9. Claims 7, 14, 22, and 25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art does not disclose or render obvious wherein an impedance discontinuity between the signal trace and the component is lowered from above 5 ohms to less than 1 ohm.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Vo (6617524) discloses electrical traces comprising of damming traces 3x's as big as the normal traces and they contain vias. Humphrey (6053751) discloses a flexible circuit that contains signal traces that have varying widths over the length of the circuit. Gilbert et al. (4551747) discloses signal traces wherein the width of the traces gets slightly greater at points where the traces emerge from under metallization areas.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Natalini whose telephone number is 571-272-2266. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, N. Le can be reached on 571-272-2233. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jeff Natalini

ANJAN DEB
PRIMARY EXAMINER